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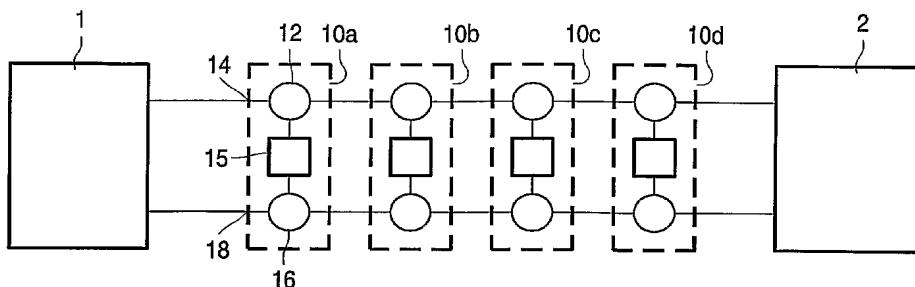
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(54) Title: ELECTRONIC CIRCUIT WITH A FIFO PIPELINE



(57) **Abstract:** An asynchronously operated FIFO pipe-line (10a-d) comprises a plurality of handshake chains functionally in parallel. Successive data items are each passed by selecting a chain dependent on a value of the data item. The FIFO pipelines (10a-d) comprise successive pipe-line stages, each pipe-line stage with respective handshake stages (12, 16) of each of the plurality of handshake chains. A coordination circuit (15) prevents handshakes in mutually different ones of handshake chains from overtaking one another. Preferably four phase handshake protocols are used with logic gates (26, 28) between the request line ((REQ1- i, REQ0- i) and the acknowledge line (ACK1- i, ACK0- i) at the input of a stage and a set-reset latch (20, 22) with a set input coupled to the output of the logic gate (26, 28). The latch has a data output coupled to the request line of at the output of the stage, a reset input coupled to the acknowledge line of the output of the stage, and a not-data output coupled to the coordination circuit (24). The coordination circuit (24) is arranged to disable response of the logic gates (26, 28) of all handshake stages in a pipeline stage while the not-data output of any one of the set-reset latches (20, 22) the pipeline stage indicates a set state.

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